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#### **Unit 3: Instruction Level Parallelism (12 Hrs)**

Instruction Level Parallelism(ILP) overview, types of hazards, Data dependencies, Name dependencies, Control dependencies, instruction scheduling, Branch instruction costs, register renaming, basic compiler technique for exposing ILP: instruction scheduling and loop unrolling, Dynamic hardware prediction, Dynamic instruction scheduling, Hardware based Speculation, Multiple Issue and static scheduling, Superscalar and VLIW or EPIC architectures, Limitations of Instruction Level Parallelism, Multithreading: thread-level parallelism to improve uniprocessor throughput. Case Study: The Intel Core i7 and ARM Cortex-A8.

#### **Unit 4: Data Level Parallelism(5 Hrs)**

Data Level Parallelism (DLP) overview, vector processors architecture, SIMD Instruction Set Extensions for Multimedia, Graphics Processing Units, Detecting and Enhancing Loop-Level Parallelism. Case study: Mobile versus Server GPUs and Tesla versus Core i7.

#### **Unit 4: Multiprocessor and Thread Level Parallelism (8 Hrs)**

Multicore processors Architectures: SIMD, MIMD, Centralized Shared Memory, Distributed shared memory architecture, Cache Coherence, directory-based coherence, Synchronization, Memory Consistency models, Case Study: Multicore Processors and Their Performance.

#### **Text Book:**

1. Hennessy J.L., Patterson D.A., Computer Architecture: A Quantitative Approach, Morgan Kaufmann, 5<sup>th</sup> edition.

#### **References:**

1. Hennessy J.L., Patterson D.A., Computer Architecture: A Quantitative Approach, Morgan Kaufmann, 4<sup>th</sup> edition.

2. David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware / Software Interface.

3. Computer architecture and embedded processor research articles and technical papers.

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The study is a non-experimental quantitative study. ... Department of Teaching and Learning and Educational Organization, University of Barcelona, ...

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